

CBT3251

1-of-8 FET multiplexer/demultiplexer

Rev. 01 — 21 December 2005

Product data sheet

1. General description

The CBT3251 is a 1-of-8 high-speed TTL-compatible FET multiplexer/demultiplexer. The low ON-resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When output enable (\overline{OE}) is LOW, the CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

The CBT3251 is characterized for operation from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

2. Features

- $5\ \Omega$ switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA

3. Ordering information

Table 1: Ordering information

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Type number	Topside mark	Package		
		Name	Description	Version
CBT3251D	CBT3251D	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
CBT3251DB	CT3251	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
CBT3251DS	CBT3251	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
CBT3251PW	CBT3251	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] Also known as QSOP16.

4. Functional diagram

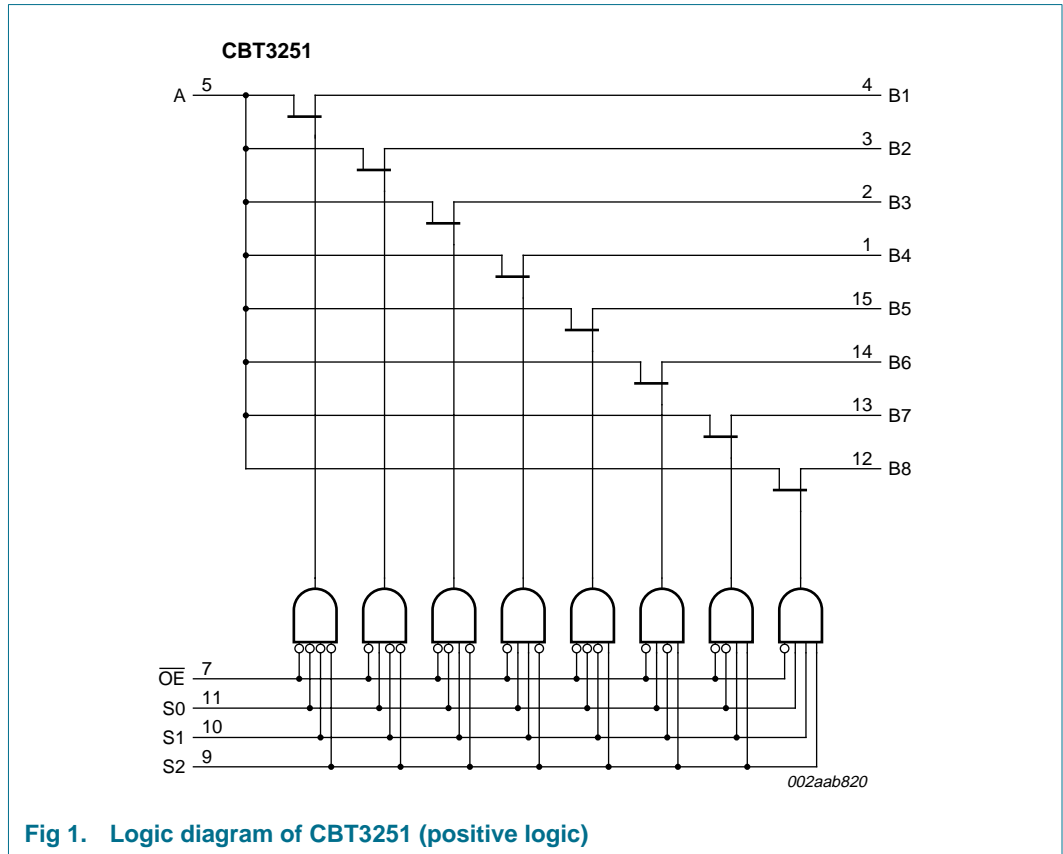
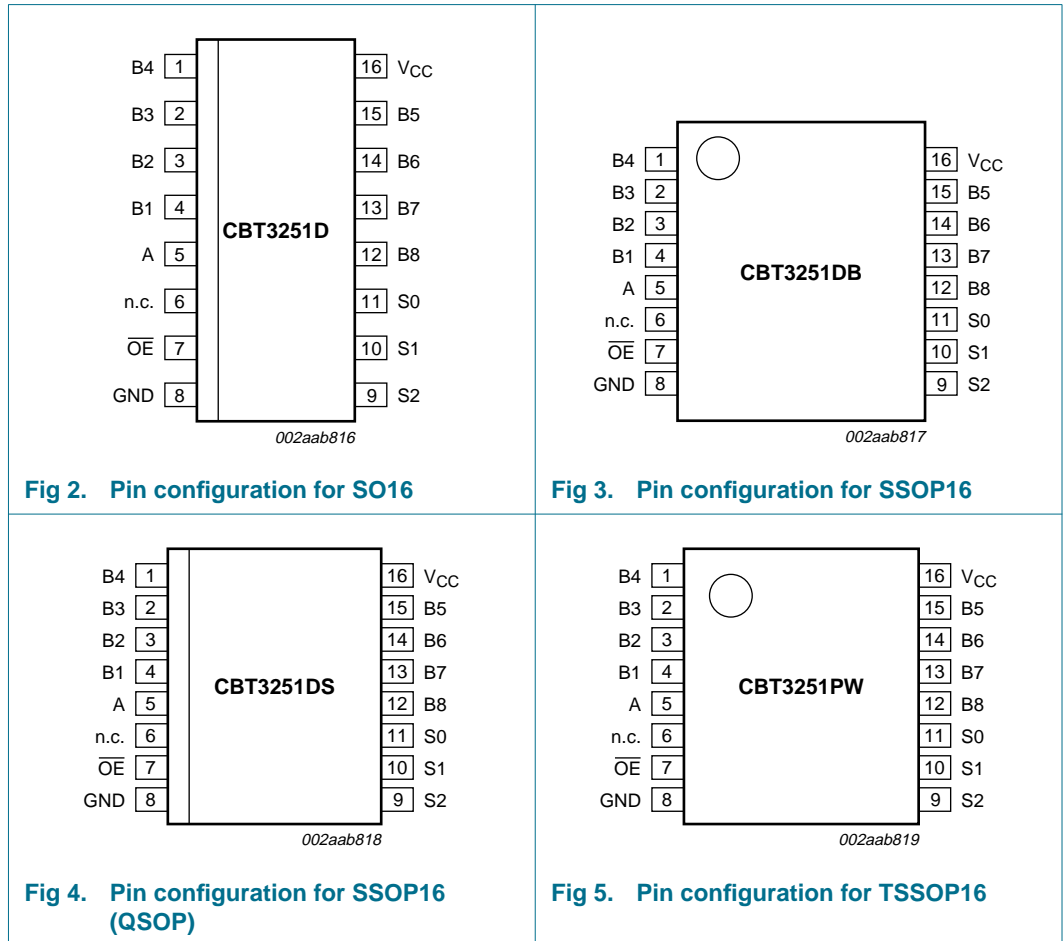


Fig 1. Logic diagram of CBT3251 (positive logic)

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
B1, B2, B3, B4, B5, B6, B7, B8	1, 2, 3, 4, 12, 13, 14, 15	B outputs [1]
A	5	A input
n.c.	6	not connected
\overline{OE}	7	output enable (active LOW)
GND	8	ground (0 V)
V _{CC}	16	positive supply voltage

[1] B outputs are inputs if A inputs are outputs.

6. Functional description

Refer to [Figure 1 “Logic diagram of CBT3251 \(positive logic\)”](#).

6.1 Function selection

Table 3: Function selection

H = HIGH state; L = LOW state; X = Don't Care.

Inputs				Function
OE	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	disconnect

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5 [1]	+7.0	V
V_I	input voltage		-0.5 [1]	+7.0	V
I_{CCC}	continuous current through each V_{CC} or GND pin		-	128	mA
I_{IK}	input clamping current	$V_I < 0$ V	-	-50	mA
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5: Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	-40	-	+85	°C

[1] All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

9. Static characteristics

Table 6: Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	$V_{CC} = 4.5\text{ V}$; $I_I = -18\text{ mA}$	-	-	-1.2	V
V_{pass}	pass voltage	$V_I = V_{CC} = 5.5\text{ V}$; $I_O = -100\text{ mA}$	3.4	3.6	3.9	V
I_{LI}	input leakage current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or 5.5 V	-	-	± 1	μA
I_{CC}	quiescent supply current	$V_{CC} = 5.5\text{ V}$; $I_O = 0\text{ mA}$; $V_I = \text{GND}$ or 5.5 V	-	-	3	μA
ΔI_{CC}	additional quiescent supply current	control inputs; $V_{CC} = 5.5\text{ V}$; one input at 3.4 V ; other inputs at V_{CC} or GND	[2] -	-	2.5	mA
C_i	input capacitance	control pins; $V_I = 3\text{ V}$ or 0 V	-	3.5	-	pF
$C_{io(off)}$	off-state input/output capacitance	A port; $V_I = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	17.5	-	pF
		B port; $V_I = 3\text{ V}$ or 0 V ; $\overline{OE} = V_{CC}$	-	4.0	-	pF
R_{on}	ON-state resistance	$V_{CC} = 4\text{ V}$; typ. at $V_{CC} = 4\text{ V}$; $V_I = 2.4\text{ V}$; $I_I = 15\text{ mA}$	[3] -	14	20	Ω
		$V_{CC} = 4.5\text{ V}$; $V_I = 0\text{ V}$; $I_I = 64\text{ mA}$	[3] -	5	7	Ω
		$V_{CC} = 4.5\text{ V}$; $V_I = 0\text{ V}$; $I_I = 30\text{ mA}$	[3] -	5	7	Ω
		$V_{CC} = 4.5\text{ V}$; $V_I = 2.4\text{ V}$; $I_I = 15\text{ mA}$	[3] -	10	15	Ω

[1] All typical values are at $V_{CC} = 5\text{ V}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND .

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

10. Dynamic characteristics

Table 7: Dynamic characteristics

$V_{CC} = +5.0\text{ V} \pm 0.5\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	propagation delay	from input (A or Bn) to output (Bn or A)	[1] -	-	0.25	ns
		from input (Sn) to output (A)	2	-	5.5	ns
t_{en}	enable time [2]	from input (Sn) to output (Bn)	1.5	-	5.6	ns
		from input (\overline{OE}) to output (A or Bn)	1.6	-	5.8	ns
t_{dis}	disable time [3]	from input (Sn) to output (Bn)	1.9	-	6.4	ns
		from input (\overline{OE}) to output (A or Bn)	2.3	-	6.2	ns

[1] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] Output enable time to HIGH and LOW level.

[3] Output disable time from HIGH and LOW level.

10.1 AC waveforms

$V_I = \text{GND to } 3.0 \text{ V.}$

t_{PLZ} and t_{PHZ} are the same as t_{dis} .

t_{PZL} and t_{PZH} are the same as t_{en} .

t_{PLH} and t_{PHL} are the same as t_{PD} .

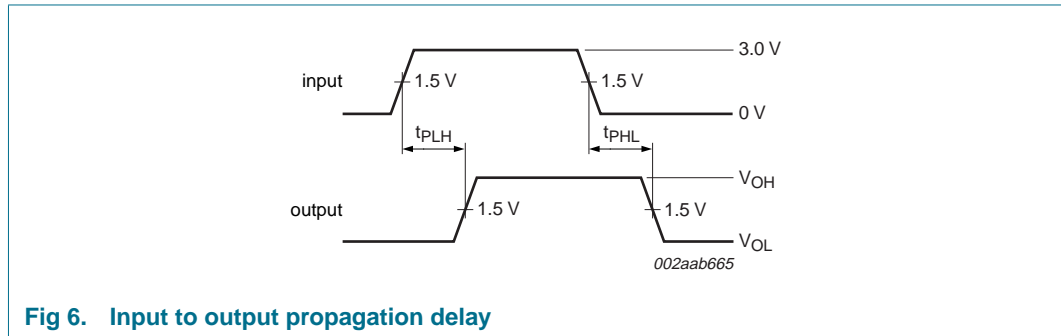
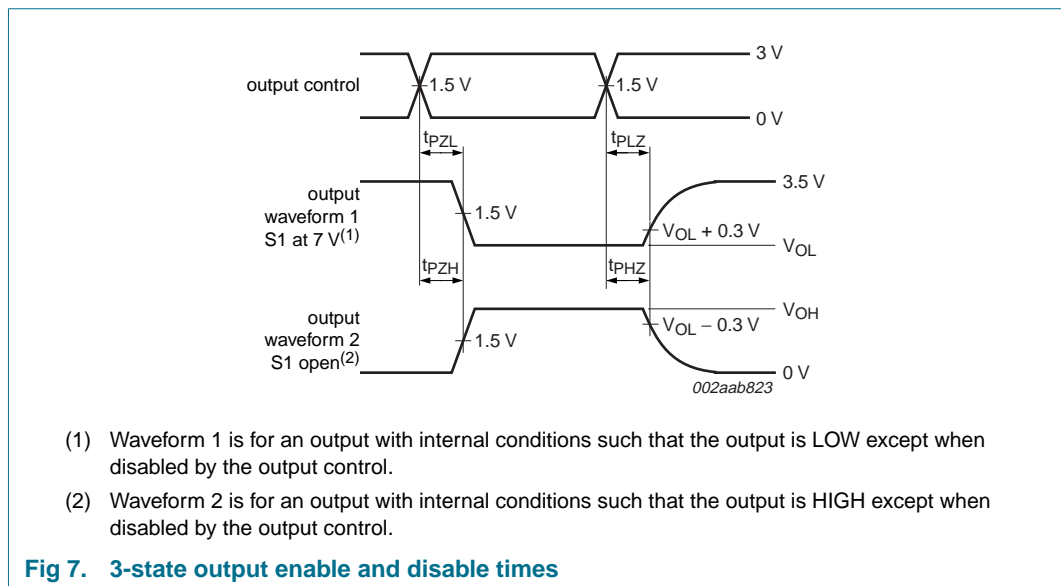


Fig 6. Input to output propagation delay



- (1) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
- (2) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 7. 3-state output enable and disable times

11. Test information

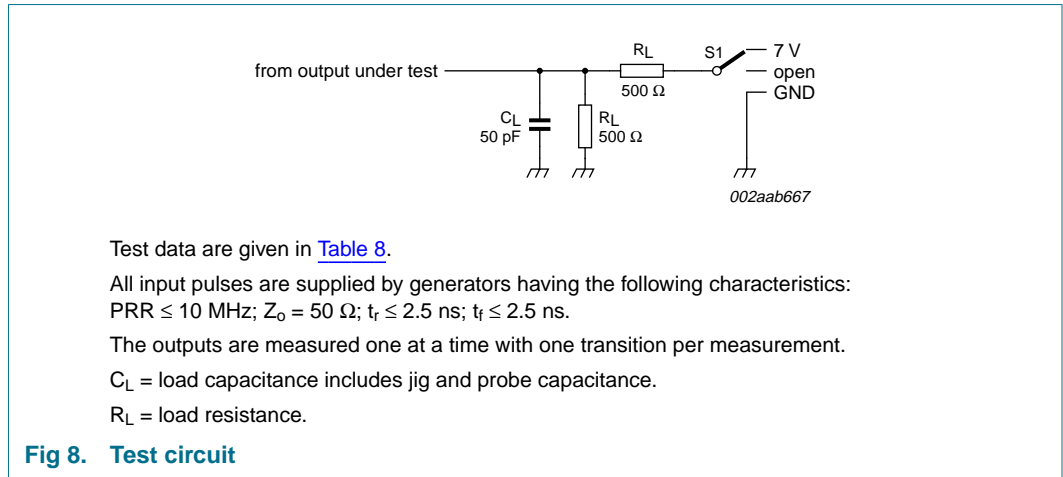


Table 8: Test data

Test	Load		Switch
	C_L	R_L	
t_{PD}	50 pF	500 Ω	open
t_{PLZ} , t_{PZL}	50 pF	500 Ω	7 V
t_{PHZ} , t_{PZH}	50 pF	500 Ω	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

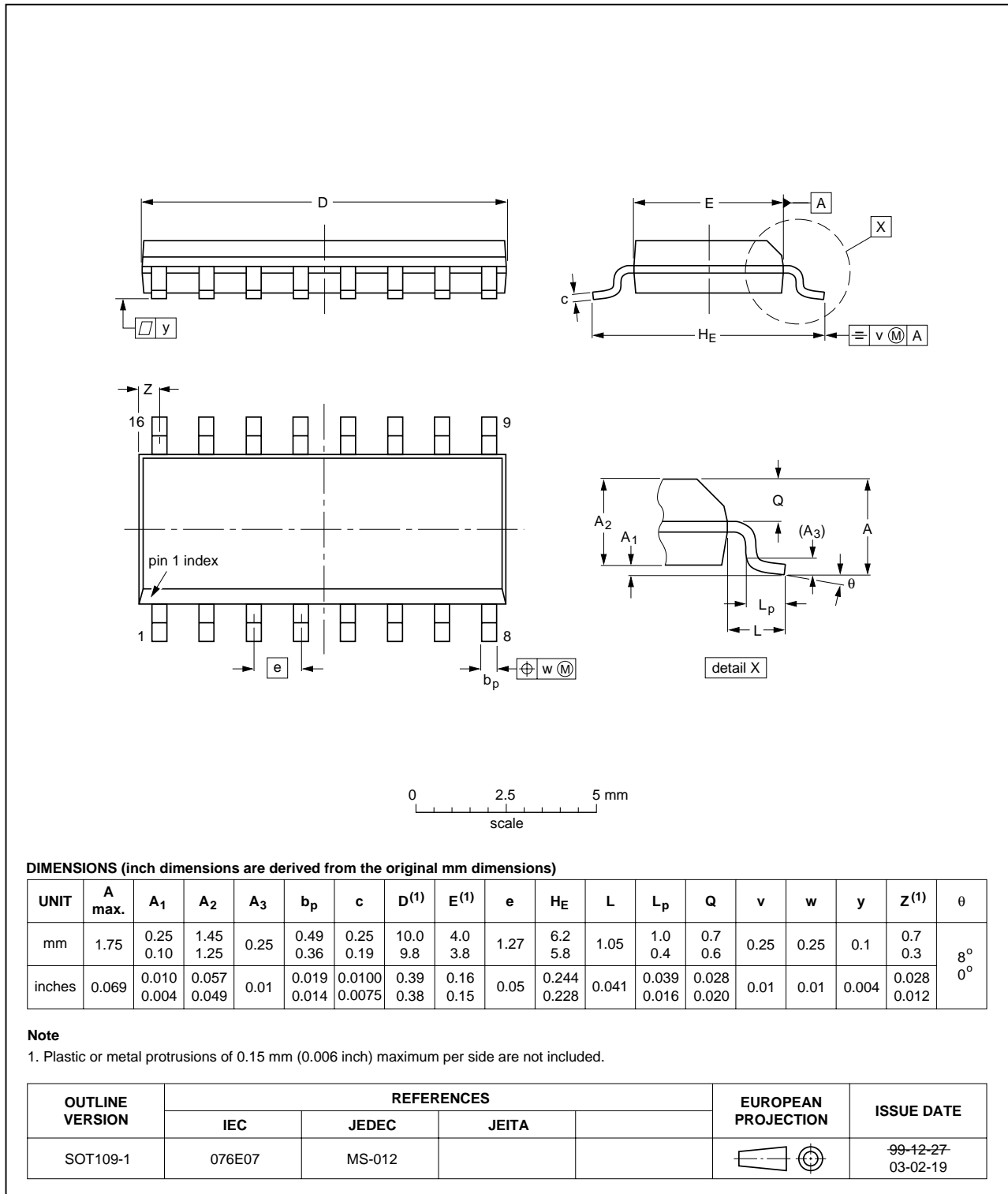


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

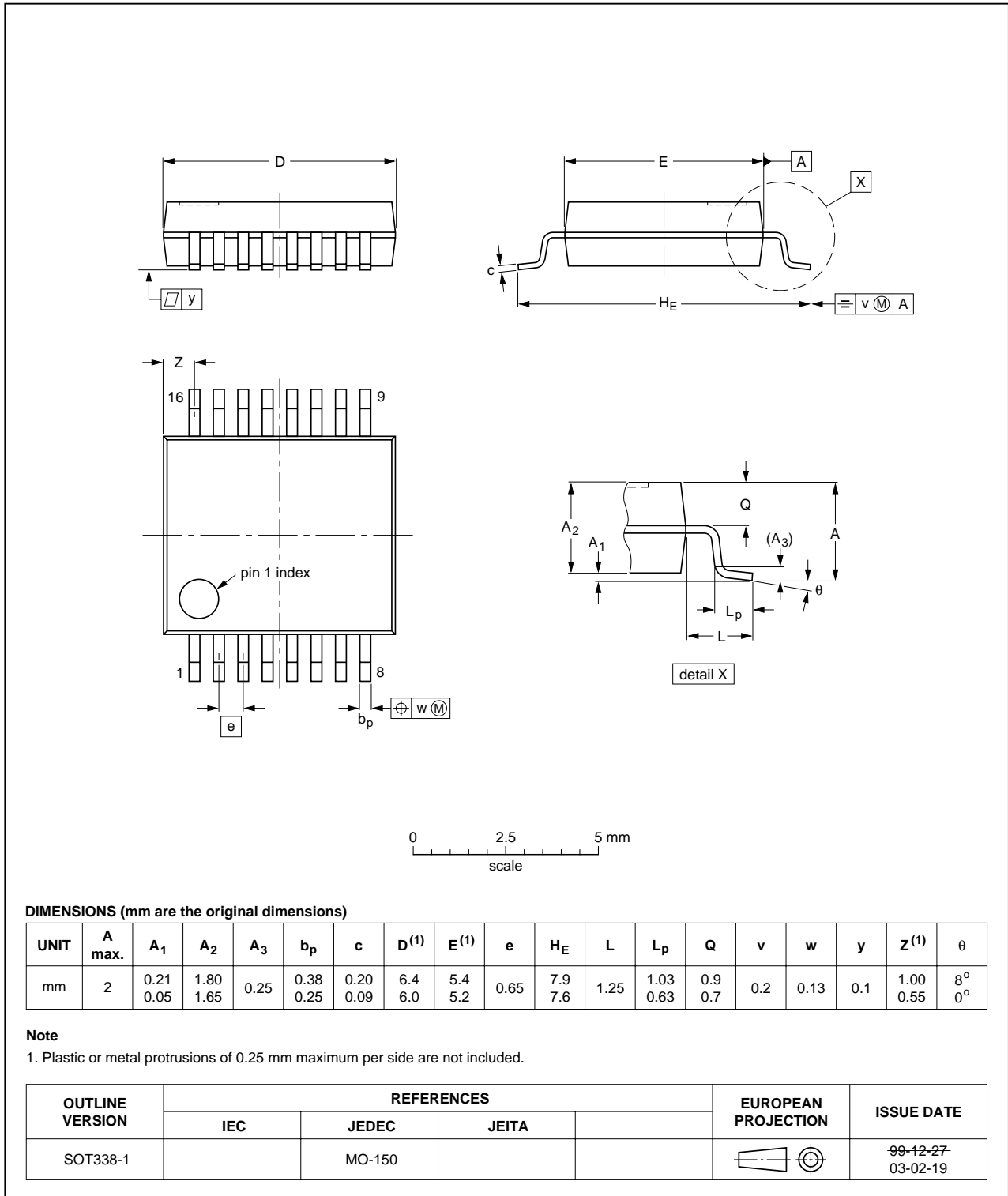


Fig 10. Package outline SOT338-1 (SSOP16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

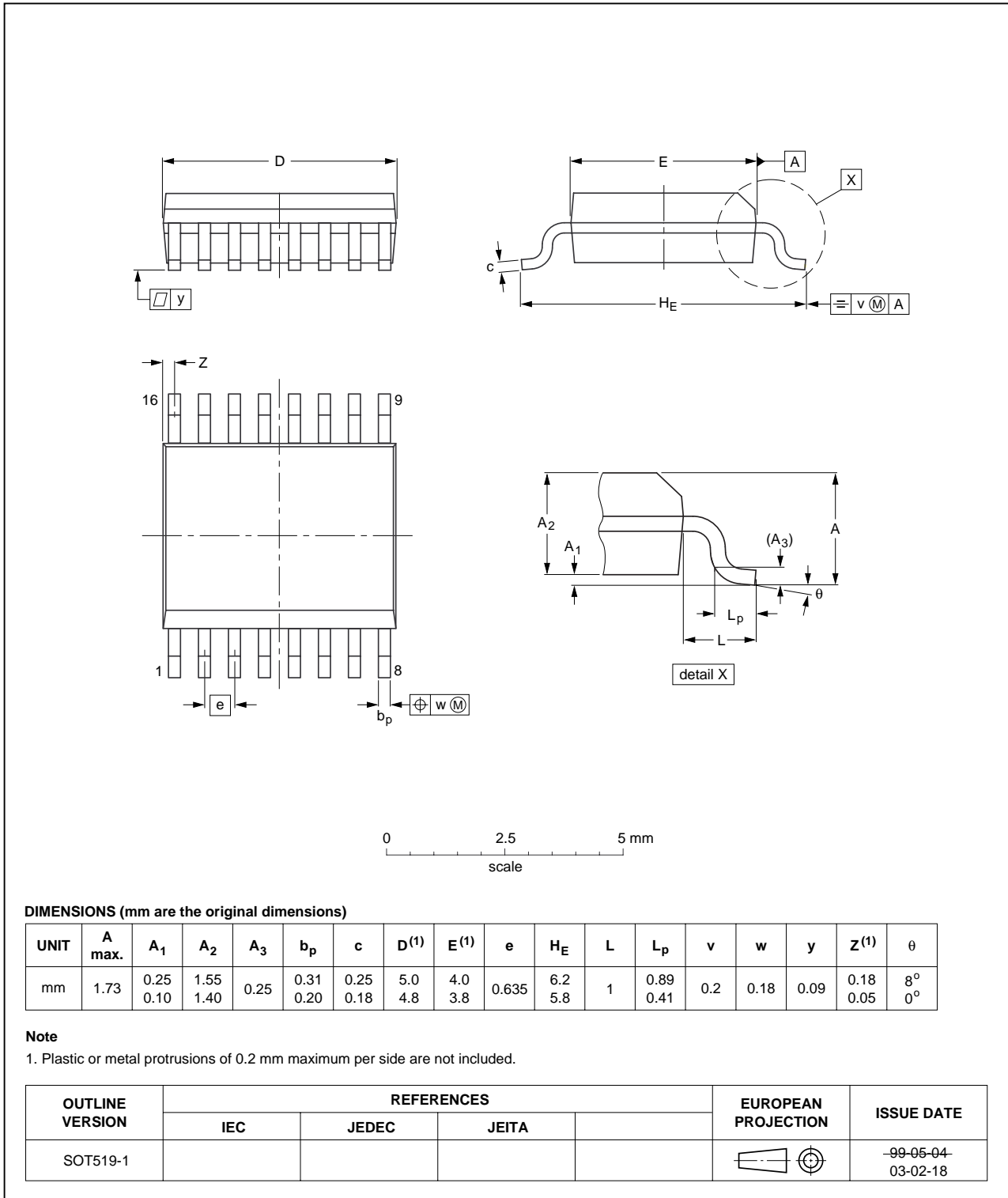


Fig 11. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

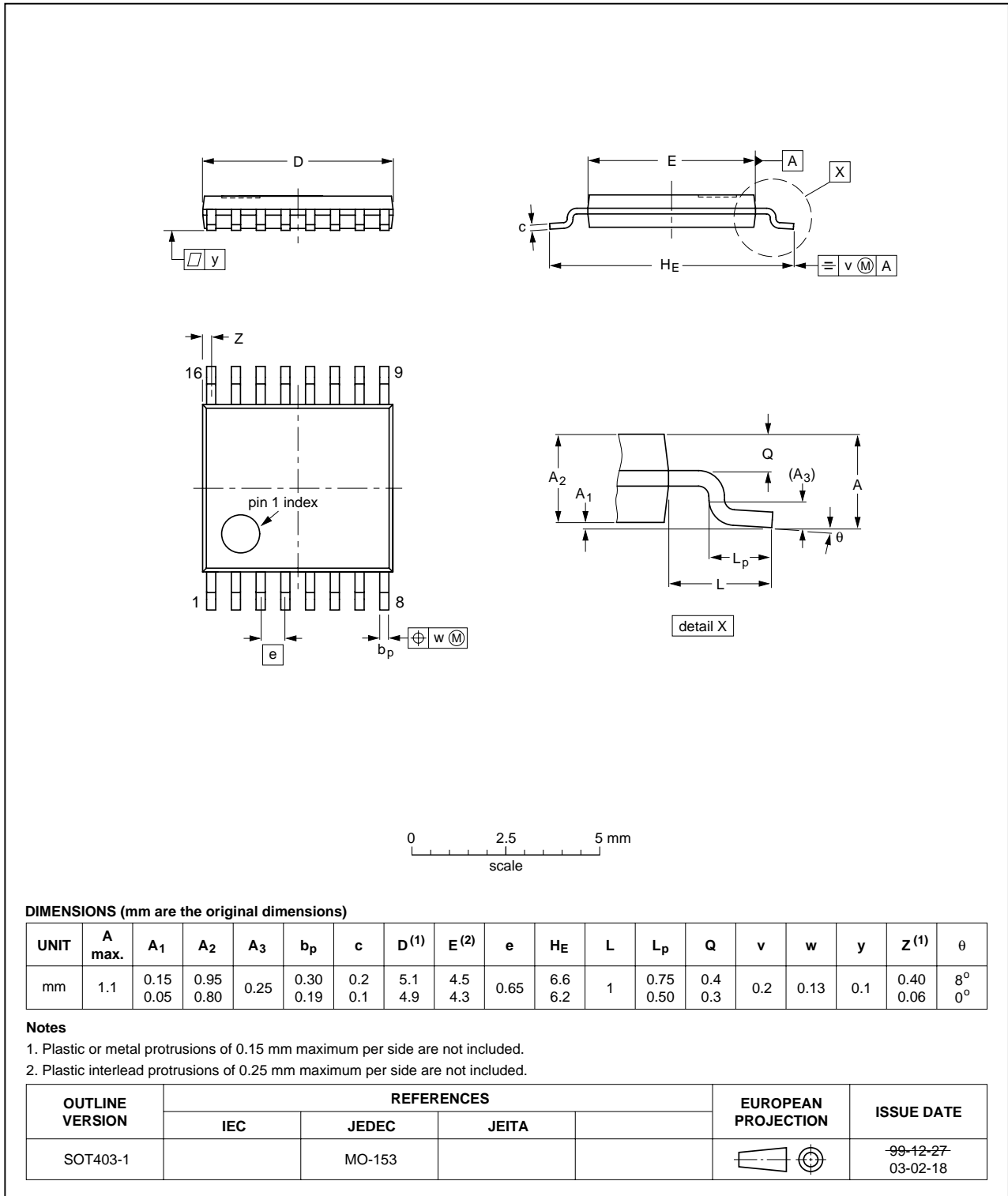


Fig 12. Package outline SOT403-1 (TSSOP16)

13. Soldering

13.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
 - for all BGA, HTSSON..T and SSOP..T packages
 - for packages with a thickness ≥ 2.5 mm
 - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note (AN01026)*; order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 10: Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
MM	Machine Model
PRR	Pulse Repetition Rate
TTL	Transistor-Transistor Logic

15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
CBT3251_1	20051221	Product data sheet	-	-	-

16. Data sheet status

Level	Data sheet status ^[1]	Product status ^[2] ^[3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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21. Contents

1	General description	1
2	Features	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	3
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	4
6.1	Function selection	4
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	5
10.1	AC waveforms	6
11	Test information	7
12	Package outline	8
13	Soldering	12
13.1	Introduction to soldering surface mount packages	12
13.2	Reflow soldering	12
13.3	Wave soldering	12
13.4	Manual soldering	13
13.5	Package related soldering information	13
14	Abbreviations	14
15	Revision history	14
16	Data sheet status	15
17	Definitions	15
18	Disclaimers	15
19	Trademarks	15
20	Contact information	15



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